12, which comprises a base layer formed of nonwoven fabric and a porous surface layer.--

--16. The polishing pad used for polishing a semiconductor wafer according to Claim 13, which comprises a base layer formed of nonwoven fabric and a porous surface layer.--

--17. The polishing pad used for polishing a semiconductor wafer according to Claim 14, wherein a content of zinc compounds in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.--

--18. The polishing pad used for polishing a semiconductor wafer according to Claim 15, wherein a content of zinc compounds in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.--

--19. The polishing pad used for polishing a semiconductor wafer according to Claim 16, wherein a content of zinc compounds in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the polishing pad.--

--20. A polishing pad used for polishing a semiconductor in a mirror polishing process, wherein it is comprises a base layer formed of nonwoven fabric and a porous surface layer, and a content of zinc compounds included in the surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the surface layer.--

--21. The polishing pad for polishing a semiconductor wafer according to claim 20, wherein the surface layer does not include zinc compounds.--

--22. The polishing pad for a semiconductor wafer according to Claim 14, wherein the surface layer is foamed of foamed polyurethane.--

--23. The polishing pad for a semiconductor wafer according to Claim 15, wherein the surface layer is foamed of foamed polyurethane.--

--24. The polishing pad for a semiconductor wafer according to Claim 16, wherein the surface layer is foamed of foamed polyurethane.--

--25. The polishing pad for a semiconductor wafer according to Claim 20, wherein the surface layer is foamed of foamed polyurethane.--